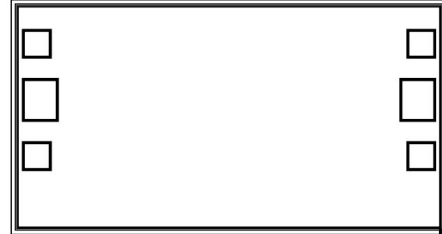


THE BIG DEAL

- 18 dB Slope
- Insertion Loss, 20.4 dB Typ. at 6 GHz
- Insertion Loss, 2.2 dB Typ. at 18 GHz
- Return Loss, 20 dB Typ.

APPLICATIONS

- Test and Measurement
- EW, Radar, and ECM Defense Systems
- Back Haul Radio



PRODUCT OVERVIEW

EQYT-18-24-D is a MMIC Gain Equalizer fabricated using highly repeatable GaAs IPD MMIC process incorporating resistors, capacitors, and inductors to accomplish a positive Insertion Loss Slope vs. Frequency. EQYT-18-24-D has a nominal Insertion Loss Slope of 18 dB across the wide bandwidth of 6 to 18 GHz and can be applied to compensate for the negative Gain Slope of amplifiers to achieve relative Gain Flatness for the overall system.

KEY FEATURES

Feature	Advantages
Positive Insertion Loss Slope vs. Frequency	Useful for compensating negative Gain Slope of amplifiers, filter effects in receivers, and transmitters to achieve Flat Gain versus Frequency.
Wideband Operation, 6 to 18 GHz	Supports a wide array of applications including Test & Measurement, EW, Radar, and ECM Defense Systems, and Back Haul radio.
Excellent Power Handling Capability	Enables its use at the output of a variety of amplifiers.
Unpackaged Die	Enable user to integrate it directly into hybrids.

ELECTRICAL SPECIFICATIONS¹ AT 25°C, 50Ω, UNLESS OTHERWISE NOTED.

Parameter	Condition (GHz)	Min.	Typ.	Max.	Units
Frequency Range		6		18	GHz
Insertion Loss	6	—	20.4	—	dB
	10	—	13.5	—	
	14	—	6.7	—	
	16	—	4.1	—	
	18	—	2.2	—	
VSWR	6 - 10	—	1.11	—	:1
	10 - 14	—	1.13	—	
	14 - 16	—	1.17	—	
	16 - 18	—	1.35	—	

1. Die is soldered in a 16L 3x3mm package and measured on Yantel Characterization Test Board TB-EQYT-18-24C. See Characterization & Application Circuit (Fig.1).

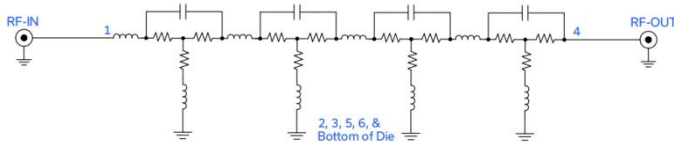
MAXIMUM RATINGS²

Parameter	Ratings
Operating Case Temperature	-55°C to +105°C
Storage Temperature	-65°C to +150°C
RF Input Power ³	+33 dBm (5 minute max) +30 dBm (continuous)

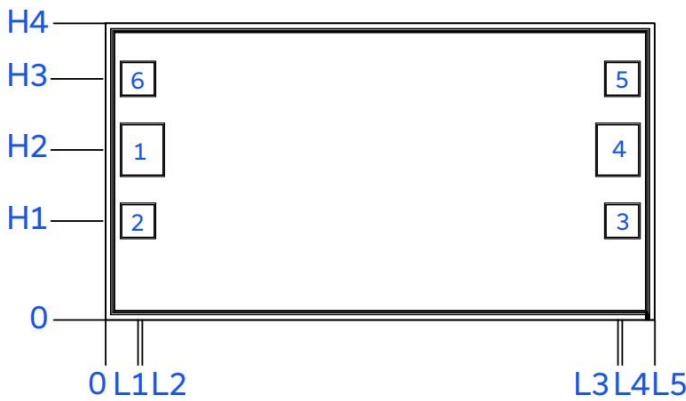
2. Permanent damage may occur if any of these limits are exceeded.

3. Derates linearly to +29 dBm at +105° C

SIMPLIFIED SCHEMATIC



BONDING PAD POSITION



Dimensions in μm, Typical

L1	L2	L3	L4	L5	H1	H2	H3	H4	Thickness	Die Size	Pad Size 1 & 4	Pad Size 2,3,5,6
92	104	1446	1459	1550	279	479	679	835	100	1550 x 835	117 x 142	92 x 92

ASSEMBLY PROCEDURE

1. Storage

Die should be stored in a dry nitrogen purged desiccators or equivalent.

2. ESD

MMIC Equalizer die are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic protected material, which should be open in clean room conditions at an appropriately grounded anti-static workstation.

3. Die Handling and Attachment

Devices need careful handling using correctly designed collets, it is recommended to handle the chip along the edges with a custom design collet. The die mounting surface must be clean and flat. Using conductive silver filled epoxy, recommended epoxies are Ablestik 84-1 LMISR4 or equivalents. Apply sufficient epoxy to meet required epoxy bond line thickness, epoxy fillet height and epoxy coverage around total periphery. Parts shall be cured in a nitrogen filled atmosphere per manufacturer's cure condition. The surface of the chip has exposed air bridges and should not be touched with vacuum collet, tweezers or fingers.

4. Wire Bonding

Bond pad openings in the surface passivation above the bond pads are provided to allow wire bonding to the die gold bond pads. Thermo-sonic bonding is used with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. Suggested wire is pure gold, 1mil diameter. Bonds must be made from the bond pads on the die to the packaged or substrate. All bond wire length and bond wire height should be kept as short as possible unless specified by the Assembly Drawing to minimize performance degradation due to undesirable series inductance.

PAD DESCRIPTION

Function	Pad Number	Description
RF-IN	1	RF-Input Pad
RF-OUT	4	RF-Output Pad
GND	2, 3, 5, 6, & Bottom of the die.	The bond pads are connected to back-side through vias and do not require wire-bond connections to ground.

CHARACTERIZATION TEST CIRCUIT

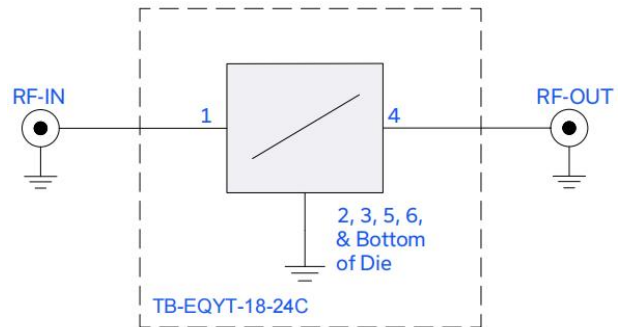


Fig 1. Characterization & Application Circuit

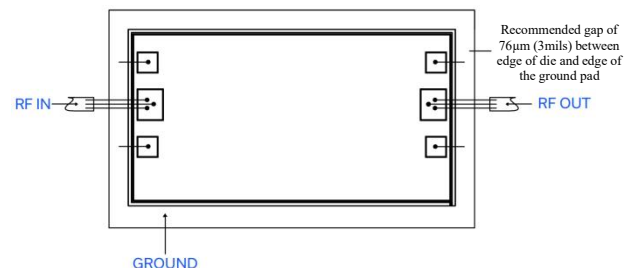
Note: This block diagram is used for characterization.

(DUT is soldered into a 16L 3x3mm package and measured on Yantel characterization test board TB-EQYT-18-24C. Insertion loss and Return Loss are measured using Keysight N5245A PNA-X Microwave Network Analyzer.

Condition:

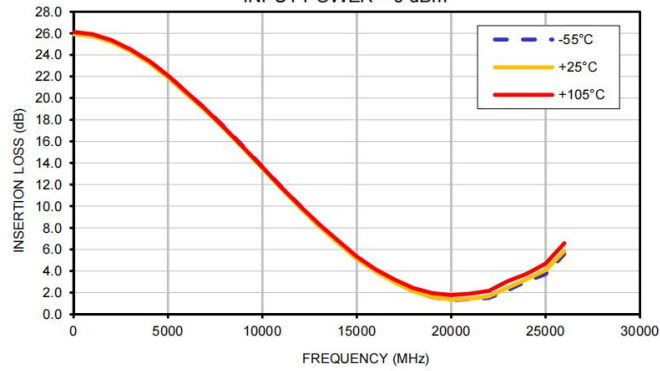
Insertion Loss & Return Loss: Pin = 0 dBm.

ASSEMBLY DIAGRAM

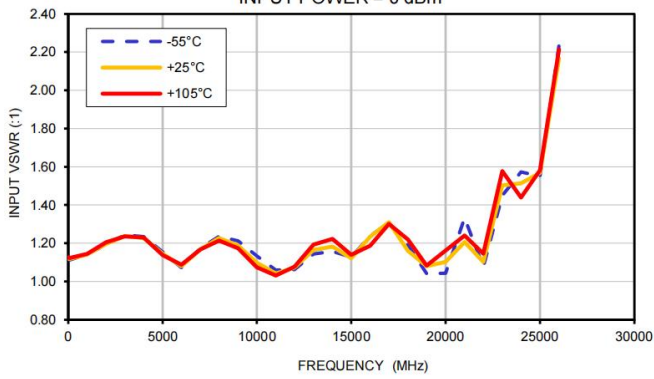


TYPICAL PERFORMANCE CURVES

INSERTION LOSS vs. TEMPERATURE
INPUT POWER = 0 dBm



INPUT VSWR vs. TEMPERATURE
INPUT POWER = 0 dBm



OUTPUT VSWR vs. TEMPERATURE
INPUT POWER = 0 dBm

